Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A scheduler for a memory system for buffer storage of data processed by at least one data processing unit, comprising:

a write unit for writing data objects to the memory system, said write unit:

receiving data packets from at least one data source at a variable data transmission rate, the data packets having payload data;

calculating attribute data for each received data packet;

writing the data contained in the data packet to the memory system as a data object string including data objects linked to one another, the data object string including pointer data for linking the data objects, the attribute data calculated, and the payload data; and

inserting filling objects into the memory system between the data objects linked to one another to compensate for

the variable data transmission rate when writing the data object string to the memory system;

a counter connected to said write unit and incremented by said write unit when the data object string is written to the memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects; ~~and~~

a time out signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value, to the data processing unit that at least one of the data object and the filling object buffer-stored in the memory system is ready to be read; and

subsequently decrementing said counter corresponding to the data contained in the data object provided[[.]];

said write unit having a control path and a data path;

said data path having a counting device incremented linearly in accordance with a linear nominal data arrival curve; and

said data path having an effective data address generator calculating a time wheel distribution as a function of a calculated cumulative amount of data and of a count produced by the counting device, as follows:

$$W^{*}_{\alpha}(t) = \begin{Bmatrix} R'(t) & \text{if } W^{*}_{\alpha}(t) > \alpha(t) \\ \max[R'(t), \alpha'(t)] & \text{if } W^{*}_{\alpha}(t) = \alpha(t) \\ \alpha'(t) & \text{if } W^{*}_{\alpha}(t) < \alpha(t) \end{Bmatrix},$$

where R(t) is an amount of data in a received data packet, and α is the linear nominal data arrival curve.

Claim 2 (original): The scheduler according to claim 1, wherein the data object string includes linked data objects having different data object types.

Claim 3 (original): The scheduler according to claim 2, wherein a first of said data object types is a string start data object having:

a type data field for identification as the string start data object;

a transmission flag;

a pointer data field for linking;

an attribute data field; and

a payload data field.

Claim 4 (original): The scheduler according to claim 2, wherein a second of said data object types is a string end data object having:

a type data field for identification as the string end data object;

a data field for inputting an amount of the payload data; and

a payload data field.

Claim 5 (original): The scheduler according to claim 2, wherein a third of said data object types is a string end and start data object having:

a type data field for identification as the string end and start data object;

a data field for outputting the amount of payload data;

a transmission flag;

an attribute data field; and

a payload data field.

Claim 6 (original): The scheduler according to claim 2, wherein a fourth of said data object types is a string center data object having:

a type data field for identification as the string center data object;

a pointer data field; and

a payload data field.

Claim 7 (original): The scheduler according to claim 2, wherein a fifth of said data object types is a single-byte filling object having a type data field including one byte for identification as a single-byte filling object.

Claim 8 (original): The scheduler according to claim 2, wherein a sixth of said data object types is a multiple-byte filling object having a type data field for identification as

a multiple byte filling object and a data field indicating an amount of filling data.

Claim 9 (canceled)

Claim 10 (original): The scheduler according to claim 9, wherein said data path has:

a FIFO memory; and

a FIFO control unit connected to said FIFO memory for writing and reading data to and from said FIFO memory.

Claim 11 (original): The scheduler according to claim 10, wherein said FIFO control unit receives data from the at least one data source in the form of packets as data packets.

Claim 12 (original): The scheduler according to claim 11, wherein each received data packet has:

a control data item identifying a start of the data packet; and

a control data item identifying an end of the data packet.

Claim 13 (original): The scheduler according to claim 12, wherein the payload data in the received data packets respectively include administration data and information data.

Claim 14 (original): The scheduler according to claim 10, wherein said FIFO control unit calculates attribute data for each received data packet.

Claim 15 (previously presented): The scheduler according to claim 14, wherein:

the payload data in the received data packets respectively include administration data; and

said control path calculates the attribute data as a function of system settings of said write unit and of the administration data in the data packets.

Claim 16 (original): The scheduler according to claim 14, wherein:

said FIFO memory has an attribute data buffer; and

said FIFO control unit buffer-stores the calculated attribute data in said attribute data buffer.

Claim 17 (original): The scheduler according to claim 10, wherein:

said FIFO memory has a payload data buffer; and

said FIFO control unit buffer-stores the payload data in a data packet with said payload data buffer.

Claim 18 (original): The scheduler according to claim 10, wherein said FIFO memory has an attribute data buffer and a payload data buffer for each data source.

Claim 19 (original): The scheduler according to claim 10, wherein:

the data source is a plurality of data sources; and

said FIFO memory has an attribute data buffer and a payload data buffer for each of the data sources.

Claim 20 (original): The scheduler according to claim 18, wherein said FIFO control unit produces an error signal when said payload data buffer associated with one data source is full and receives no further data.

Claim 21 (original): The scheduler according to claim 10, wherein:

said control path transmits control signals to said FIFO control unit; and

said FIFO control unit writes the attribute data and the payload data of a data packet to the memory system in the form of a data object string including data objects linked to one another as a function of the control signals said FIFO control unit receives from said control path.

Claim 22 (original): The scheduler according to claim 10, wherein said FIFO control unit records a cumulative amount of attribute data of the attribute data in a data packet.

Claim 23 (original): The scheduler according to claim 10, wherein said FIFO control unit records the cumulative amount of payload data of the payload data in a data packet.

Claims 24 - 25 (canceled)

Claim 26 (currently amended): The scheduler according to claim [[~~25~~]]1, wherein:

said data path has a modulo-M adder; and

said modulo-M adder adds a cumulative amount of attribute data to the calculated time wheel distribution[[+]] to produce a data object address modulo-M, where M is a memory capacity of the memory system.

Claim 27 (currently amended): The scheduler according to claim [[9]]1, wherein:

said data path has a basic address register bank including at least two basic address registers; and

one of said basic address registers is provided for each data source.

Claim 28 (currently amended): The scheduler according to claim [[9]]1, wherein:

the data source is a plurality of data sources;

said data path has a basic address register bank including at least two basic address registers; and

one of said basic address registers is provided for each of said data sources.

Claim 29 (currently amended): ~~The scheduler according to claim 27, wherein:~~ A scheduler for a memory system for buffer storage of data processed by at least one data processing unit, comprising:

a write unit for writing data objects to the memory system, said write unit:

receiving data packets from at least one data source at a variable data transmission rate, the data packets having payload data;

calculating attribute data for each received data packet;

writing the data contained in the data packet to the memory system as a data object string including data objects linked to one another, the data object string including pointer data for linking the data objects, the attribute data calculated, and the payload data; and

inserting filling objects into the memory system between the data objects linked to one another to compensate for

the variable data transmission rate when writing the data object string to the memory system;

a counter connected to said write unit and incremented by said write unit when the data object string is written to the memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects;

a time out signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value, to the data processing unit that at least one of the data object and the filling object buffer-stored in the memory system is ready to be read; and

subsequently decrementing said counter corresponding to the data contained in the data object provided;

said write unit having a control path and a data path;

said data path having a basic address register bank including at least two basic address registers; and

one of said basic address registers being provided for each data source; and

said data path ~~has~~having:

a FIFO memory; and

a FIFO control unit connected to said FIFO memory for writing and reading data to and from said FIFO memory;

said FIFO control unit records the cumulative amount of payload data of the payload data in a data packet; and

an initial address of the data object is written to said basic address register whenever there is a change to the calculated cumulative amount of payload data.

Claim 30 (currently amended): The scheduler according to claim [[~~9~~]]1, wherein:

said data path has a link address register bank including at least two link address registers; and

one of said link address registers is provided for each data source.

Claim 31 (currently amended): The scheduler according to claim [[~~9~~]]1, wherein:

the data source is a plurality of data sources;

said data path has a link address register bank including at least two link address registers; and

one of said link address registers is provided for each of said data sources.

Claim 32 (original): The scheduler according to claim 30, wherein said link address register buffer-stores an address of the data object written most recently to the memory system for linking to a next data object in the data object string.

Claim 33 (original): The scheduler according to claim 10, wherein said data path has a data multiplexer for writing data to the memory system and an address multiplexer for supplying an address to the memory system.

Claim 34 (currently amended): ~~The scheduler according to claim 33, wherein:~~ A scheduler for a memory system for buffer

storage of data processed by at least one data processing unit, comprising:

a write unit for writing data objects to the memory system, said write unit:

receiving data packets from at least one data source at a variable data transmission rate, the data packets having payload data;

calculating attribute data for each received data packet;

writing the data contained in the data packet to the memory system as a data object string including data objects linked to one another, the data object string including pointer data for linking the data objects, the attribute data calculated, and the payload data; and

inserting filling objects into the memory system between the data objects linked to one another to compensate for the variable data transmission rate when writing the data object string to the memory system;

a counter connected to said write unit and incremented by said write unit when the data object string is written to the

memory system to correspond to an amount of data contained in the data packet and the filling data in the filling objects;

a time out signaling unit connected to said counter, said time out signaling unit:

signaling, when said counter reaches a threshold value, to the data processing unit that at least one of the data object and the filling object buffer-stored in the memory system is ready to be read; and

subsequently decrementing said counter corresponding to the data contained in the data object provided;

said write unit having a control path and a data path;

said data path having:

a FIFO memory; and

a FIFO control unit connected to said FIFO memory for writing and reading data to and from said FIFO memory;

said data path having a data multiplexer for writing data to the memory system and an address multiplexer for supplying an address to the memory system;

said data path ~~has~~ having a basic address register bank including at least two basic address registers;

one of said basic address registers is provided for each data source; and

said data multiplexer ~~has~~having:

a first input connected to said FIFO memory, said first input receiving the attribute and payload data read from said FIFO memory; and

a second input connected to said base address register bank, said second input receiving the linking data.

Claim 35 (original): The scheduler according to claim 34, wherein:

said data path has a data multiplexer for writing data to the memory system and an address multiplexer for supplying an address to the memory system;

said data path has a link address register bank including at least two link address registers;

one of said link address registers is provided for each data source;

said modulo-M adder has an output; and

said address multiplexer has:

a first input connected to said output of said modulo-M adder, said first input receiving a data address from said output; and

a second input connected to said link address register bank, said second input receiving a string address from said link address register bank.

Claim 36 (original): The scheduler according to claim 26, wherein:

said data path has a data multiplexer for writing data to the memory system and an address multiplexer for supplying an address to the memory system;

said data path has:

a FIFO memory; and

a FIFO control unit connected to said FIFO memory for writing and reading data to and from said FIFO memory;

said data path has a link address register bank including at least two link address registers;

one of said link address registers is provided for each data source;

said modulo-M adder has an output; and

said address multiplexer has:

a first input connected to said output of said modulo-M adder, said first input receiving a data address from said output; and

a second input connected to said link address register bank, said second input receiving a string address from said link address register bank.

Claim 37 (original): The scheduler according to claim 35, wherein:

said control path generates a control signal;

said data path is switched between first and second operating modes as a function of said control signal;

said first input of said data multiplexer and said first input of said address multiplexer are each connected to the memory system in said first operating mode to write data objects to the memory system; and

said second input of said data multiplexer and said second input of said address multiplexer are each connected to the memory system in said second operating mode to link a most recently written data object.

Claims 38 - 39 (canceled)